Please substitute the following paragraph that begins on Page 10, line 12 and ends on Page 10, line 21 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

Memory cell 202C also includes storage capacitor 219 for storing data in the cell. A first plate of capacitor 219 for memory cell 202C is integral with [second] first source/drain region 210 of access transistor 211. Thus, memory cell 202C may be more easily realizable when compared to conventional vertical transistors since there is no need for a contact between [second] first source/drain region 210 and capacitor 219. Second plate 220 of capacitor 219 is common to all of the capacitors of array 200. Second plate 220 comprises a mesh or grid of n+ poly-silicon formed in deep trenches that surrounds at least a portion of [second] first source/drain region 210 of each pillar 204A through 204D. Second plate 220 is grounded by contact with substrate 212 underneath the trenches. Second plate 220 is separated [from] first source/drain region 210 by gate oxide 222.

Please substitute the following paragraph that begins on Page 11, line 1 and ends on Page 11, line 7 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

Figure 4 is a schematic diagram that illustrates an effective circuit diagram for the embodiment of Figures 2 and 3. It is noted that storage capacitor 219 formed by [second] first source/drain region 210 and second plate 220 is depicted as four separate capacitors. This represents that the [second] first plate 220 surrounds second source/drain region 210 which increases the charge storage capacitance and stored charge for the memory cell. It is also noted that second plate 220 is maintained at a constant potential, e.g., ground potential.